

**MADANAPALLE INSTITUTE OF TECHNOLOGY AND SCIENCE, MADANAPALLE- 517 325**  
**DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING – Time Table for 2024-25**  
**M.TECH I SEMESTER**

**Class In Charge:** Dr. Vivek Jain

**With effect from:** 17/10/2024

**Class Room:** EB – 218A

DAY/TIME	10.10-11.10	11.10 -12.10	12.10-01.10	1.10 – 2.00	2.00 – 3.00	3.00 – 4.00	4.00 – 5.00
<b>MON</b>	LP-VLSI	RM	CMOS	<b>B R E A K</b>	MC & PDSP	Holistic Activities	
<b>TUE</b>	FPGA	LP-VLSI	RM		<b>CMOS LAB</b>		
<b>WED</b>	RM	CMOS	DM		<b>MC &amp; PDSP LAB</b>		
<b>THU</b>	MC & PDSP	LP-VLSI	FPGA		DM	Holistic Activities	
<b>FRI</b>	DM	CMOS	FPGA		MC & PDSP	Holistic Activities	
<b>SAT</b>	Holistic Activities				Holistic Activities		

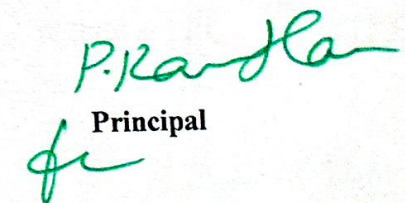
<b>THEORY</b>			
	<b>CODE</b>	<b>SUBJECT</b>	<b>NAME OF STAFF MEMBER</b>
CMOS	24VESP101	CMOS Digital IC Design	Dr. Vivek Jain
MC & PDSP	24VESP102	Microcontrollers and Programmable Digital Signal Processors	Dr. S. Rajasekaran
FPGA	24VESP403	FPGA Architectures and Applications	Mr. Chandramouli Joshi
LP-VLSI	24VESP404	Low Power VLSI Design	Dr. G. Reddy Hemantha
RM	24RMP101	Research Methodology and IPR	Dr. Agnibha Das Majumdar
DM	24AUP901	Disaster Management	Dr. Priyam Nath Bhowmik
<b>LABORATORY</b>			
CMOS lab	24VESP201	CMOS Digital IC Design Laboratory	Mr. H. Shree Kumar & Mr. V. Mustafa
MC & PDSP Lab	24VESP202	Microcontrollers and Programmable Digital Signal Processors Laboratory	Dr. S. Rajasekaran & Mr. Y. Pradeep Kumar



Time Table coordinator



HOD



Principal